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FreeRTOS-SMP Debugging

- RR Rohith R
- **Forum name:** #Debugging

Hi Team,

I am trying to debug FreeRTOS-SMP on quad core using Trace 32.

(i) I want to know How can I see the registers of all the 4 cores at a time?

(ii) Also How can I debug (step into the codes) all the 4 cores at the same time .

To do all these what changes I have to do in the .cmm file

Comments (5)

Khaled Jmal

3 months ago

Hello Rohit,

first, you use an SMP CPU selection in TRACE32 PowerView. If you can give me more information about your target processor, then I could help you more with this.

Please then have a look to "SMP Concept" and "Basic Debugging (SMP)" in

https://repo.lauterbach.com/pdf/training_debugger_smp.pdf

RR Rohith R

3 months ago

My target processor contain 4 A53 core. So that I have to run the code on all this 4 cores. I can load and run the program but i don't know on which core the code is running. I want to view the registers of all cores as a part of debug. I need 4 debug windows ,one for each core

so that when i step in the code i can see it on all the 4 cores. Here I am adding some portion of my .cmm file.

```
SYStem.CPU XXXX
SYStem.CONFIG CORE 1. 1.
CORE.ASSIGN 1. 2. 3. 4.
*****
Data.LOAD.Elf "xxx_smp.elf" ;.out smp file for 4 core
Register.Set PC _init_/CORE 1.
Register.Set PC _init_/CORE 2.
Register.Set PC _init_/CORE 3.
Go _init_
Mode.Hll
WinPOS 0. 0. 116. 26.
List.auto
```

By this code a single window with _init_ code portion will come.It may be the 4th core.

Khaled Jmal

3 months ago

You need to open a List window with the /CORE option:

```
List.auto /CORE 0
List.auto /CORE 1
List.auto /CORE 2
List.auto /CORE 3
```

RR Rohith R

3 months ago

I have tried with this. Now I can see the code snippet and registers of all the 4 cores at the same time. But Now there is a problem when debugging, step in it is not properly step in all the 4 core simultaneoulsy. Is it the issue with .cmm file?

RR Rohith R

3 months ago

Also

```
List /CORE
Register.view /CORE
Go __system_start
```

```
List /CORE 1.
Register.view /CORE 1.
Go __system_start
```

List /CORE 2.

Register.view /CORE 2.

Go __system_start

List /CORE 3.

Register.view /CORE 3.

Go __system_start

When I use this code snippet to debug from __system_start in all the 4 cores, core1, core2 and core3 is available. Core 0 __system_start and its registers are not available.