



[Knowledgebase](#) > [FAQs by core architecture](#) > [ARC](#) > [\[ARC\] Error message "debug port fail"](#)

[ARC] Error message "debug port fail"

2025-09-16 - [Comments \(0\)](#) - [ARC](#)

The error "debug port fail" can happen with TRACE32 for ARC under the following circumstances:

- Stopping the core on **SYStem.UP** failed, because the core does not stop even after 1000ms.
Try **SYStem.Mode Attach** instead of **SYStem.Mode Up**
- The JTAG Status Register of the ARC debug interface reports an error, by showing the Failure-Bit active.
Try a lower JTAG frequency (e.g.: **SYStem.JtagClock CTCK 1MHz**).
- A read or write transaction to/from the ARC core does not complete. The JTAG Status Register does not show the Ready bit after waiting for 1000ms and even not after re-initializing the read/write-transaction and waiting for. Try a lower JTAG frequency (e.g.: **SYStem.JtagClock CTCK 1MHz**).
Disable or disconnect any external source which resets the ARC core frequently (like e.g. a watchdog timer).