[ARC] Error message "debug port fail"

2026-08-13 - Comments (0) - ARC
Note

This FAQ describes the cause of the **"debug port fail"** error for the **ARC** architecture.

If you are looking for information about this error on an **Arm** target, please refer to [Arm] SYStem.Up / SYStem.Attach returns "debug port fail"

The error message **"debug port fail"** can occur with TRACE32 for ARC under the following circumstances:

- **The core cannot be stopped during** `SYStem.UP`**.**
  TRACE32 attempts to stop the core for up to 1000 ms, but the core does not stop.
  Try using `SYStem.Mode Attach` instead of `SYStem.Mode Up`.

- **The ARC debug interface reports an error.**
  The JTAG Status Register of the ARC debug interface indicates an error by setting the Failure bit.
  Try reducing the JTAG clock frequency, for example:

  ```
  SYStem.JtagClock CTCK 1MHz
  ```

- **A read or write transaction to or from the ARC core does not complete.**
  The JTAG Status Register does not indicate the Ready bit within 1000 ms. Re-initializing the read/write transaction and waiting another 1000 ms does not resolve the problem either.
  Try reducing the JTAG clock frequency, for example:

  ```
  SYStem.JtagClock CTCK 1MHz
  ```

  Also, disable or disconnect any external source that frequently resets the ARC core, such as a watchdog timer