

## Which setup/hold times can be provided by the TRACE32 tools for JTAG?

2024-05-23 - Comments (0) - TRACE32 PowerView

### Note

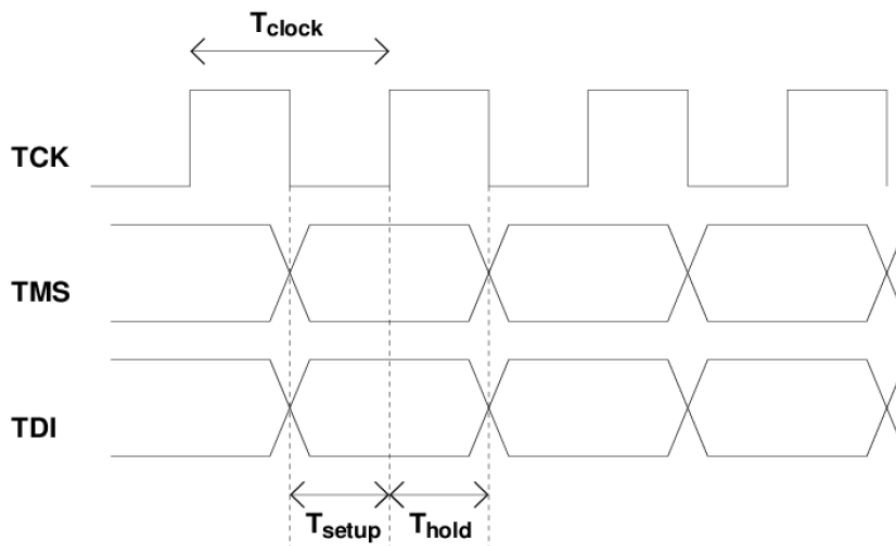
This article uses a simplified representation of the timings (for example any kind of jitter and skew is ignored). This is reasonable because all timings depend on a configurable JTAG TCK clock frequency; to increase the margin to cover skew, jitter etc. Simply use a lower JTAG TCK clock frequency.

For JTAG ports, the debugger sends three signals to the target chip for communication via JTAG:

- **TCK** : Clock signal, driven by the debugger.
- **TMS** : Signal driven by the debugger to control the JTAG TAP Controller.
- **TDI** : Signal driven by the debugger to send data into the target chip.

The debugger changes the value of the **TMS** and **TDI** signals coincident to the falling edge of **TCK**.

So the **TMS** and **TDI** signals have the following timing relative to **TCK** :



The target chip should sample the **TMS** and **TDI** signal on the rising edge of **TCK**.

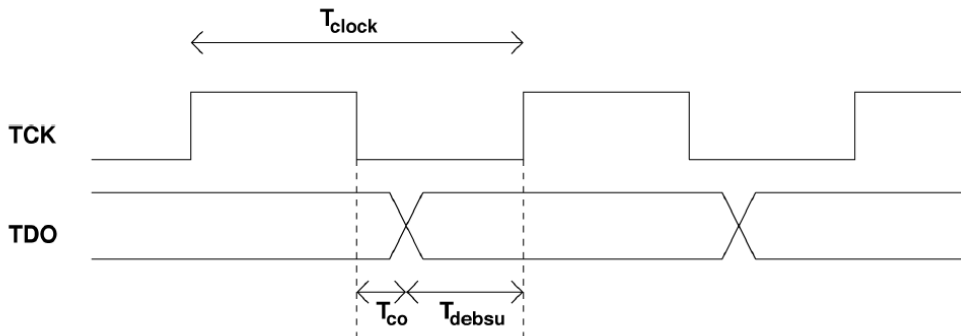
For the target chip this means that the debugger will produce a setup (**Tsetup**) and hold time (**Thold**) of half the cycle time (**Tclock**) of TCK.

### Example

At a TCK frequency of 1Mhz (**Tclock** = 1us), **Tsetup** = 500ns and **Thold** = 500ns.

The target chip drives the signal. The value of the signal should change after the falling edge of **TCK**. The target chip has an implementation dependent clock to output timing (**Tco**).

According to the JTAG specifications, the debugger should sample the **TDO** signal on the rising edge of **TCK**:



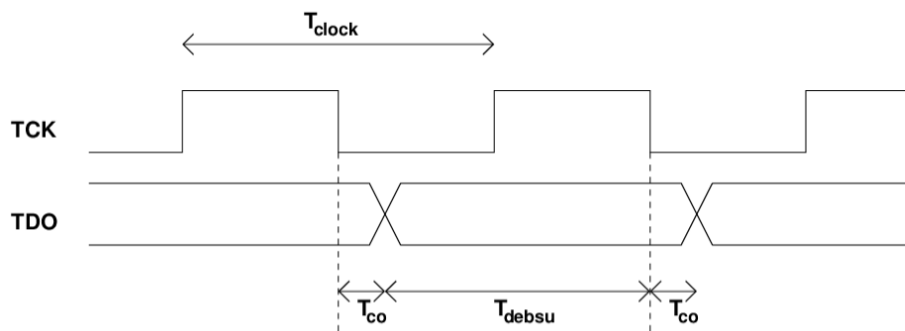
For the debugger this means the target chip will generate data on the **TDO** signal with a setup time of **Tdebsu** =  $T_{clock}/2 - T_{co}$ . The hold time of the data will be  $T_{co} + T_{clock}/2$ .

### Example

At a TCK frequency of 1MHZ (**Tclock** = 1us) and **Tco** = 10ns => **Tdebsu** = 490ns.

The debugger has the requirement that  $T_{co} + T_{clock}/2 > 0$ ns (hold time requirement) and **Tdebsu** > 7.5ns (setup time requirement).

For some processor architectures, including Arm, the debugger samples the **TDO** signal on the **falling** edge of TCK. This allows to achieve higher TCK frequencies (which means lower **Tclock** values). In this case the following picture explains the timing:



So in this case the target generates a setup time for the debugger of **Tdebsu** =  $T_{clock} - T_{co}$ .

The debugger still has a 0 ns hold time requirement, so in this case it must hold that  $T_{co} >$

0ns.

**Summary:**

Any setup/hold time requirements can be met by lowering the JTAG frequency. If you know which setup/hold time requirements for your chip, then you can deduct the maximum reachable JTAG frequency.