[PowerArchitecture] SYStem.Option.FREEZE influence on timers/counters

2022-01-14 - Comments (0) - PowerQUICC III (internal / reps)

The **SYStem.Option.FREEZE** setting just uses the debug related registers to influence the timer / counter behavior when the target enters the debug halted state.

QorIQ CPUs typically offer an additional register in the RCPM, called CTBHLTCR or TTBHLTCR.

If the corresponding bit for a specific core in this register

- is set to 1, the **SYStem.Option.FREEZE** setting can handle both: To let the timers run or to freeze them during the core is in the debug halted state.
- is set to 0, the timers will always be frozen in the debug halted state, regardless of the **SYStem.Option.FREEZE** setting.