[TriCore] Why does a hot attach to my AURIX device fail, whereas it succeeds only when preceded by SYStem.Up?

2026-10-05 - Comments (0) - TriCore

If a hot attach using `SYStem.mode Attach` only succeeds after performing a `SYStem.Up` (which triggers a reset), it is likely due to one of the following reasons:

1. A mismatch between the configured protocol in the debugger and the mode the TriCore device enters at startup

For TriCore devices, the debug protocol is determined by the state of the TRST signal at the moment the RESET line transitions from low to high:

- A TriCore device will be in DAP mode if **TRST was high** at the time **RESET** was released.
- A TriCore device will be in JTAG mode if **TRST was low** at the time **RESET** was released.

Since release R.2018.02, `SYStem.CONFIG.DEBUGPORTTYPE DAP2` is the default debugger configuration. If the target is configured to enter JTAG mode, a direct `SYStem.mode Attach` will fail because the debugger is configured to use the DAP protocol.

To allow hot attach, you must ensure the debugger and the device are using the same protocol. You can do this:

- Either by connecting TRST- to a pull-up resistor to force the device into DAP mode at startup.
- Or by configuring the debugger to use JTAG mode via `SYStem.CONFIG.DEBUGPORTTYPE JTAG`

For more details, refer to the section **"Debug Interface Configuration"** in app_tricore_ocds.pdf.

See also the FAQ [TriCore] Which Debug Protocol should I use: DAP or JTAG?

2. The debug interface is locked

In case the debug interface of the device is locked, and a password must be provided via `SYStem.Option.KEYCODE` there is only a short time window at startup where the debugger can communicate with the startup software (SSW) to unlock the debug interface. Thus, connection is only possible via commands that involve a reset, i.e., `SYStem.Mode Up` or `SYStem.Mode Go`, or during reconnection using `SYStem.Mode STANDBY`.

3. The application fails to start up without the debug module enabled

This issue is often caused by the internal watchdog timer. By default, the TriCore watchdog timer is disabled when OCDS is enabled (i.e., when the debugger is attached).
If the internal watchdog triggers a reset at user code startup due to an inappropriate watchdog timer configuration, the target application will enter a continuous reset loop. In this state, attempting to connect via hot attach will likely result in a “debug port fail” error.

This can be verified as follows:

- Set `SYStem.Option.WDTSUS ON`. This will cause the watchdog timer to start and stop with the CPU.
- Connect using `SYStem.Mode Up`, then start the CPU with `Go.direct`.

If a reset occurs, the internal watchdog timer configuration in the application code must be investigated.