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## We debug two chips over two JTAG connector with two debug modules. Is it possible to stop both chips synchronously?

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You can use the **sYnch** window, then the synchronization is done by software with about a millisecond delay.

B::SYnch		- • •
synch     OFF	Connect	
O ON RESet	(not connected to other instances)	
	MasterGo MasterBreak MasterStep MasterSystemMode	slave SlaveGo SlaveBreak SlaveStep SlaveSystemMode

Otherwise, you can get a hardware-based synchronization if the chip supports BDGREQ and DBGACK signals. In this case, you can connect both debug modules over PODBUS and use the commands **TrBus.Out Break ON** and **TrBus.Set Break ON** for each PowerView instance. This type of synchronization is however not supported for synchronous start (**Go**).

- <b>T</b> - B::TrBus		
- control	Connect	- Set (from BUS)
OFF	<ul> <li>Out</li> </ul>	🖂 Break
Arm	◯ln	ABreak
- level	- Mode	ATrigger
high	• Low	
- monitor	◯ High	Out (to BUS)
	O 📉 Falling	🗹 Break
- Trigger	○ <u> </u>	ABreak
Trigger		ATrigger

Refer for more information to the documentation of these commands in <u>General Commands</u> <u>Reference Guide T</u>.